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EXAMINER

NELSON, ALECIA DIANE

ART UNIT PAPER NUMBER

2675

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/834,919

Applicant(s)

AKIMOTO ET AL.

Examiner

Alecia D. Nelson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 August 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 April 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "21" (Figure 1) and "22" (specification) have both been used to designate the data line. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. ***Claims 1-27 and 29-38*** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s),

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at the time the application was filed, had possession of the claimed invention.

Independent **claims 1, 29, 31, 32, 33, and 35-37** no require that the device has a plurality of memory elements for storing *digital* display data, however there is no disclosure in the specification as originally filed that describes this limitation. At most claim 28 as originally filed states that the image signal generating means outputs an image signal based on digital display data. However this is not sufficient disclosure to the new limitation requiring that the memory elements store digital display data. **Claims 2-27, 30, 34, and 38** are rejected for being dependent on a rejected base claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

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Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 1, 9, 11, 14-17, 21-23, 25, and 29-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,627,557) in view of Booth, Jr. et al., hereinafter Booth (U.S. Patent No. 6,642,915).

With reference to the **claim 1**, Yamaguchi et al. teaches a matrix of pixels (11 a) is disposed in the liquid crystal panel (11), wherein each pixel (11 a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 6719). A plurality of memory elements (sample hold circuit) for storing ^{digital} display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 46-55), wherein there is applied a refresh signal (see Fig. 16).

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Booth teaches a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element (120), a circuit that stores a charge that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123) includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data. Booth also teaches that each storage unit (124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125) (see column 5, lines 6-42).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device similar to that which is taught by Yamaguchi et al. which suggest usage of a refreshing signal in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display device that which the responding property of the liquid crystal is prevented from degrading.

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With reference to **claim 9**, Yamaguchi et al. teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

With reference to **claim 11**, Yamaguchi teaches that the other end of the memory capacitor is connected to a wire to which a preset voltage (5) is applied.

With reference to **claims 12-14**, Yamaguchi teaches that the other end of the memory capacitor is connected to a drain of the amplifier (see Figures 1-2).

With reference to **claim 15**, Yamaguchi teaches that the drain of the amplifier FET is connected to a voltage applying means (GND) (see Figures 1-2).

With reference to **claim 16**, Yamaguchi teaches that the source of the amplifier is connected to the voltage applying means (see Figure 1-2).

With reference to **claims 17 and 25**, Yamaguchi teaches that the plurality of basic units of the memory elements are connected to the data lines, and the amplifier FET is connected to the data line through a switch (1).

With reference to **claims 21-23**, Yamaguchi fails to specifically teach that the memory elements are arranged in a matrix along a group of data lines extending in a y-direction, wherein the memory switch and the selection switch in

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the individual units are connected to the same data line or data lines different from each other. Yamaguchi does teach that the pixels are arranged in a matrix and wherein elements (14, 15) have a single connection line that passes through each of the pixel elements. Moreover it is taught that the circuit structure of each pixel is not limited to the disclosed structure but includes the circuit structures according to other examples (see Fig. 14, column 15, lines 10-19).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the data line to connect both the memory switch and selection switch as taught by in by Yamaguchi or allow the memory switch and the selection switch to be connected to data lines different from each other as suggested by the teachings of Yamaguchi in order to provide a connection to the elements which allows the overall device to operated more efficiently.

With reference to **claim 26**, Yamaguchi et al. and Booth fail to specifically teach that the image signal generating means comprises a DIA converter. However it is well known in the art for the data driver to include a DIA converter.

With reference to **claims 29-31 and 36-38**, Yamaguchi et al. teaches a matrix of pixels (11 a) is disposed in the liquid crystal panel (11), wherein each pixel (11 a) is provided with a switching element. A scanning signal line driver (18) and data signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a

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group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

With further reference to **claims 32-35**, Yamaguchi et al. teaches amplifying a voltage level of the display data written in the data line and then rewriting the amplified voltage of the display data from the data line (see column 7, lines 25-34).

Yamaguchi et al. fails to specifically teach a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. However, Yamaguchi does teach that timing is controlled to refresh each pixel so as to display an image based on a new data signal (see column 16, lines 4655), wherein there is applied a refresh signal (see Fig. 16). Yamaguchi et al. fails to specifically teach refreshing by sequentially scanning, however this is a well-known scanning technique.

Booth teaches a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element 9120), a circuit that stores a charge that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123)

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includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data. Booth also teaches that each storage unit (124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125) (see column 5, lines 6-42).

Therefore it would have been obvious to one having ordinary skill in the art to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth, in a device similar to that which is taught by Yamaguchi et al. which suggest usage of a refreshing signal in order to remove any remaining charge or, in the case of gradation displays, remove any gradation from the pixel before applying the new gradation signal. This would thereby provide a display device that which the responding property of the liquid crystal is prevented from degrading.

7. **Claims 2-8, 10, 18-20, 24, and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. and Booth as applied to **claim 1** above, and further in view of Parks (U.S. Patent No. 5,471,225).

With reference to **claims 2**, Yamaguchi et al. teaches a driving circuit (20) which is disposed in the peripheral portion of the liquid crystal panel (11) (see column 16, line 2-5).

Yamaguchi et al. and Booth fail to specifically teach that the liquid crystal region is formed between the pixel electrodes and the counter electrode,

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however it is inherently known that the liquid crystal is located in such position to those skilled in the art.

Parks teaches the general construction of the LCD consisting of a pair of glass plates (22, 24), wherein the inside surface of glass panel (22) is a common electrode (30) and the inside of glass panel (24) is a pixel electrode wherein the liquid crystal (40) is located there between.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 3**, Yamaguchi et al. and Booth also fail to teach that the plurality of display pixels have an optical reflecting plate, however this to is well known in the art.

Parks teaches that the usage of alignment coatings and/or passivity coatings, are generally placed between electrode (30) and liquid crystal medium (40) as well as between each display electrode and liquid crystal medium.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of

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different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 4**, Yamaguchi et al. teaches that the LC panel (11) occupies a display portion including a scanning signal and data signal line driver can be included in the display portion as shift registers (14, 15) and timing generating circuit (17) (see column 16, lines 12-17) thereby reducing the area need for the components, and in turn allowing the display area to be made smaller.

With reference to **claims 5 and 18-20**, Yamaguchi et al. teaches with reference to conventional art that the switching elements are TFTs (see column 1, lines 8-17).

With reference to **claims 6-8 and 10**, Yamaguchi teaches that the memory capacitor (CH) is a capacitor between a gate and a channel of the amplifier (see Figures 1-2).

Even though Yamaguchi et al. and Booth fail to teach that the switch or amplifier is of Poly-Si TFT type, the usage of such type TFT is well known in the art. Booth does teaches that the storage unit (124) may include a transistor that is activated to couple the capacitor to the pixel cell to refresh the terminal voltage across the pixel cell (see column 5, lines 33-38).

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Parks teaches that the gate of the TFT is deposited upon the substrate accordingly to the well-known methods (see column 6, lines 36-52).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the conventional structure of the LCD panel to be used as suggest by Yamaguchi et al., Booth, and Park in order to provide an optimum display device which can be operated under a plurality of different driving schemes thereby not requiring a new arrangement of the display device when a new driving scheme is employed.

With reference to **claim 24**, Yamaguchi et al. and Booth fail to specifically teach a black matrix shielding means arranged between the transparent substrate corresponding to the back portions of the memory element and a lighting means. However, the usage of a black matrix is well known in the art.

With reference to **claim 27**, Yamaguchi et al. and Booth fail to specifically teach that the image signal generating means comprises a DIA converter. However it is well known in the art for the data driver to include a DIA converter.

8. **Claim 28** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Zhang et al. (U.S. Patent No. 6,611,261).

With reference to **claim 28**, Yamaguchi et al. teaches a matrix of pixels (11a) is disposed in the liquid crystal panel (11), wherein each pixel (11a) is provided with a switching element. A scanning signal line driver (18) and data

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signal line driver (19) are arranged to drive image signals to generate an image by writing the image signal to the display pixels through a group of signal lines and pixel switches (column 15, lines 67-19). A plurality of memory elements (sample hold circuit) for storing display data including a memory switch (1), a memory capacitor (CH) connected to the memory switch; an amplifier FET (2) of which a gate is connected to the memory capacitor (see column 6, lines 47-63).

Yamaguchi et al. fails the specific usage of an image signal generating means, which has a reference voltage generating circuit using a poly-Si thin film resistor as a gray scale voltage generating resistor.

Zhang et al. teaches a LCD device wherein it is disclosed the conventionality of using poly-silicon thin film transistors in LCD units and the peripheral circuits as well (see column 1, lines 15-20). It is further taught the usage of a D/A converter (350), which is comprised in the poly-Si digital driver, for generating gray scale signals based on the gray-scale reference voltage (see column 15, lines 42-57).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the combination of the poly-Si type image signal generating means as taught by Zhang et al. to be used in a device similar to that which is taught by Yamaguchi et al. in order to provide an improved arrangement for peripheral circuits of the display unit thereby allowing them to be formed as an integrated device.

Response to Arguments

Applicant's arguments filed 8/9/04 have been fully considered but they are not persuasive. The applicant argues with reference to **claims 1, 28, 29, 31, 36 and 37** that the combination of Yamaguchi and Booth fails to teach the claimed limitations including a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor. The applicant states Yamaguchi discloses a display apparatus wherein a refresh is used to clear previous data, which has been read out from the image element capacitor. The applicant also states that Booth teaches storage units to regularly refresh the pixel cells automatically without receiving new image data. However the applicant believes that this is different from a refreshing operation means for performing a operation to rewrite a signal charge stored in the memory capacitor as recited in the claims. The examiner fails to see the difference in the claimed subject matter and the teaching of the combined references. The data stored in the memory element is refreshed, meaning that the data is changed from that which was initially stored. Therefore if the stored data of Yamaguchi is cancelled, cleared, or deleted, the data is changed from that which is initially stored thereby refreshing the stored data. The applicant also argues intended usage of the refreshing operation in Booth, however intended usage is not being examined only the claimed limitations. Dependent **claims 2-8, 10, 18-20, and 24** are argued with relation to **claim 1**. The rejection to **claim 28** has been changed due to the amendment of the claim.

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Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (703) 306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
February 19, 2005

AMR A. AWAD
PRIMARY EXAMINER

